

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	210	(717/144).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:11
S2	2	S1 and pipelining and parallelizing	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:13
S3	63	compiler and pipelining and parallelizing	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:13
S4	37	compiler and pipelining and parallelizing and network	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:13
S5	16	compiler and pipelining and parallelizing and network and intel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:22
S6	8	d-stage near2 pipeline	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2007/05/31 12:29
S7	2	("6418528").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/31 12:32

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S8	2	("6324643").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/05/31 13:49
S9	2	("6651246").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/01 10:00
S10	2	("20050108696").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/01 11:48
S11	3	("6804634").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/06/01 11:48
S12	2	("7272596").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/12/10 13:03
S13	2	("20030061262").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/12/10 13:04

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pipelined FPGA applications

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Results 1 - 10 of about 518,000 for **[pipelined FPGA applications](#)**. (0.28 seconds)**Search Space Properties for Mapping Pipelined FPGA Applications ...**

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Coarse-Grain **Pipelined FPGA Applications**. Heidi Ziegler, Mary Hall, and Byoungro So.

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now be **pipelined** in the **FPGA** (the same technique that the. DSP uses for standard functions), ... **applications**, including those shown in Figure 3. Image pro- ...

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creating efficient **HPC/FPGA applications** and likely ... For example, (**pipelined**) stages of. a computation can have drastically different operat- ...

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**pipelined** adders and fits into one Atmel. AT6010 **FPGA**. We will also discuss how.

CacheLogic .... solutions to low-budget procedural **applications**. In areas ...

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mapping coarse-grain **pipelined applications** to **FPGAs** at the Workshop for Languages and Compilers for. Parallel Computing (LCPC03) in October. ...

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the performance of system-level **applications** in **FPGAs**, as ... be implemented as 4

**pipelined** 8-bit adders. Inputs to LUTs ...

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